

REMARKS

In the Office Action dated September 17, 2003, claims 1-15 are noted as pending. Claims 1-4 and 13-15 are rejected under 35 USC 102(b) as being anticipated by Saulsbury et al., U.S. Patent No. 6,128,702 (hereinafter Saulsbury). Claims 5-8 are rejected as being unpatentable over Saulsbury in view of Westberg et al., U.S. Patent No. 5,361,391 (hereinafter Westberg). Applicant requests cancellation of claims 2, 10, and 13-15. Reconsideration of the application is respectfully requested.

Objections to the Specification

The specification has been amended to cure the informality.

REJECTIONS UNDER 35 U.S.C. 102(b) and 103(a)

Neither Saulsbury, nor Westberg, either alone or in combination, disclose a data cache located on a memory module controlled by a command sequencer and serializer unit in a memory controller where the memory controller and memory module are coupled together via a memory bus as claimed in amended claim 1. It should be noted that the command sequence and serializer unit and array of tag addresses are not located on the memory module, as indicated by the language of claim one describing a memory bus coupling the memory controller the memory module.

Claims 5 and 9 similarly include limitations where the array of tags are located in a memory controller and the data cache is located on a memory module.

For these reasons, claims 1, 3-9, and 11-12 are patentable over the Saulsbury and Westberg references.

CONCLUSION:

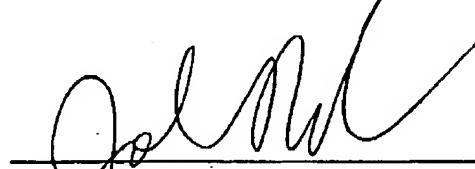
In view of the foregoing, Applicant submits that claims 1, 3-9, and 11-12 are distinguished over the cited art and are in condition for allowance. Allowance of claims 1, 3-9, and 11-12 is respectfully requested.

DEPOSIT ACCOUNT AUTHORIZATION

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any additional charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP



John Patrick Ward
Reg. No. 40,216

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12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1030
(408) 720-8598